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THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A system comprising:

a processor;

a detector to detect a power management event; and

a controller to transition, in response to the power management event, a first setting of the processor from a first performance mode to a second performance mode, including to raise a processor supply voltage level from a first voltage level to a second voltage level, and then to raise the processor clock frequency from a first frequency level to a second frequency level, the processor to remain in an active mode during the voltage level transition, wherein during the frequency level transition the processor is to be placed in a sleep state ~~of~~ and not a deep sleep state, a core processor clock remains active during the sleep state.

2.-6. (Canceled)

7. (Previously presented) The system of claim 4, wherein a system clock input to the processor remains active during the sleep state.